AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application:

Listing of Claims:

1. (Currently amended) A self-testing random access memory (RAM) system for a computer, comprising:

a memory array; ~~and~~

a self-testing RAM interface that includes a microprocessor, the self-testing RAM interface is embedded on a circuit board with the memory array and tests integrity of data stored in the memory array;

the self-testing RAM interface with the memory array and a central processing unit (CPU) of the computer are formed on separate integrated circuits and the self-testing RAM interface cooperates with the CPU to facilitate testing memory array data cells by dividing the memory array, so that each of the CPU and the microprocessor concurrently test the array thus facilitating faster testing of the memory array.

2. (Previously Presented) The system of claim 1, the self-testing RAM interface interacts with the central processing unit (CPU) to test the CPU to memory interface.

3. (Cancelled)

4. (Original) The system of claim 1, the self-testing RAM interface can correct errors in data stored in the memory array.

5. (Original) The system of claim 4, the self-testing RAM interface corrects errors by replacing erroneous data with redundant data stored in the memory array.

6. (Cancelled)

7. (Previously Presented) The system of claim 1, the self-testing RAM interface includes a memory component that facilitates execution of testing and/or correcting algorithms.

8. (Original) The system of claim 1, the self-testing RAM interface is implemented with discrete logic.

9. (Original) The system of claim 1, the self-testing RAM interface is implemented using SoC (System on Chip) technology.

10. (Original) The system of claim 1, the memory array is associated with a field programmable gate array.

11. (Original) The system of claim 1, the self-testing RAM interface is constructed with higher performance memory devices than the memory array including Gallium Arsenide based devices.

12. (Original) The system of claim 1, the self-testing RAM interface comprises large geometry devices and ECC, wherein the large geometry and ECC make the RAM interface less susceptible to errors than the memory array.

13. (Original) The system of claim 1, the self-testing RAM interface supports multiport memory access.

14. (Currently amended) A self-testing and self-validating memory system comprising:

one or more memory storage banks;

at least one central processing unit (CPU) with a self-testing RAM interface subsystem for ensuring correct data retrieval; and

a second microprocessor embedded in a single circuit board with the memory banks, the CPU and the memory banks are embedded in separate circuit boards; the self-testing RAM interface subsystem cooperates with the CPU to facilitate testing memory storage banks by dividing the memory storage banks, so that the CPU and the microprocessor concurrently test the memory storage banks thus facilitating faster testing of the memory storage bank.

15. (Original) The system of claim 14, the storage banks comprising standard RAM components with internal flaws.

16. (Original) The system of claim 14, the self-testing RAM interface is constructed with higher performance memory devices than the memory array including Gallium Arsenide based devices.

17. (Original) The system of claim 14, the self-testing RAM interface comprises large geometry devices and ECC, wherein the large geometry and ECC make the RAM interface less susceptible to errors than the memory storage banks.

18. (Original) The system of claim 14, the self-testing RAM interface acts as a virtual memory manager and maps received data to multiple copies of the data in different memory banks to enable correct data retrieval.

19. (Original) The system of claim 18, error correction codes (ECCs) and voting mechanisms determine the most probable data value to return from amongst the multiple copies.

20. (Currently amended) A self-correcting and self-validating RAM device comprising:

a plurality of internal memory stores ;

at least one central processing unit (CPU); ~~and~~

a microprocessor embedded with the memory stores on a circuit board; and

a self-testing interface that includes the microprocessor and maps input addresses and data to a multitude of memory cells on a plurality of memory stores to facilitate accurate data storage and retrieval, wherein the memory cells store copies of the input data and the self-testing interface cooperates with the CPU to facilitate testing memory stores by dividing the memory stores, so that each of the CPU and the microprocessor concurrently test the stores thus facilitating faster testing of the memory stores.

21. (Original) The device of claim 20, error correction codes (ECCs) and voting mechanisms determine the most probable data value to return from amongst the plurality of stored copies.

22. (Currently amended) A method whereby a memory device tests itself comprising:

writing values to one or more memory cells in a memory device;

reading the values stored by the one or more memory cells;

comparing the values written with the values read; ~~and~~

notifying a central processing unit if any of the values written differ from the values read, wherein writing values, reading a value, comparing values, and notifying a central processing unit are performed by a self-testing RAM interface, the self-testing RAM interface further comprising a microprocessor, the self-testing RAM interface is embedded with the memory cells on a single circuit board; and

testing the one or more memory cells by dividing the memory cells, so that the CPU and the self testing RAM interface concurrently test the cells thus facilitating faster testing of the memory cells.

23. (Original) The method of claim 22, the values written correspond to a test pattern.

24. (Original) The method of claim 22, the central processing unit is notified by generating an interrupt.

25. (Cancelled)

26. (Original) The method of claim 22, further comprising bringing the memory device on-line for use upon successful test completion.

27. (Original) An article of manufacturing comprising a computer usable medium having computer readable stored instructions thereon to perform the method of claim 26.

28. (Currently amended) An article of manufacturing comprising a computer usable medium having computer readable instructions stored thereon to perform a method for testing a central processing unit (CPU) to memory interface comprising:

loading a data pattern into CPU registers;

writing the pattern from the registers to at least a portion of memory in a memory device;

reading the data written to each memory cell;

comparing the data written with the data expected in accordance with the pattern; and

notifying the CPU if any data read is different than the data expected, wherein reading the data, comparing the data, and notifying the CPU are performed by a self-testing RAM interface; ~~and~~

embedding a second microprocessor ~~embedded~~ in a single circuit board with the memory device, the CPU and the memory device are formed of different integrated circuits; and

dividing memory cells on the memory device so that the CPU and the second microprocessor concurrently test the cells thus facilitating faster testing of the memory cells.

29. (Cancelled)

30. (Currently amended) A method for detecting hard errors comprising:

writing a test pattern to a plurality of memory cells in a memory device;

reading the value of each memory cell containing a portion of the test pattern;

comparing the value read with the value written to each cell;

recording the number times the value written did not correspond to the value read for each cell, wherein writing a test pattern, reading the value, comparing the value, and recording the number of times the value written did not correspond to the value read are performed by a self-testing RAM interface and controlled at least by a microprocessor integrated with the self-testing RAM interface and the self-testing RAM interface with the microprocessor is embedded in the memory device; and

facilitating faster detection of hard errors by dividing the memory cells, so that the CPU and the microprocessor concurrently test the cells..

31. (Original) The method of claim 30, further comprising:

determining whether any cell or cells have produced erroneous results more than a threshold number of times;

determining whether any extra memory cells are available; and

mapping any cells that have produced erroneous results more than a threshold number of times to available extra memory cells.

32. (Original) The method of claim 31, further comprising notifying an exception handler if there are no available extra cells.

33. (Original) The method of claim 30, wherein data regarding the number of times a cell value did not correspond to the value read is stored in a memory component located within the self-testing RAM interface.

34. (Currently amended) A method of reading data from a self-testing RAM device comprising:

choosing a memory address;

retrieving data from a memory location associated with the address;

determining whether the data is correct;

correcting the data if it is incorrect; ~~and~~

outputting the data to the requesting device, wherein the method disclosed hereby is performed by a self-testing RAM interface;

the self-testing RAM interface further comprises a microprocessor, and the interface is part of a circuit board that includes the memory location; and

dividing a memory device including the memory address, so that each of the CPU and the microprocessor concurrently test the memory device.

35. (Original) The method of claim 34, wherein the self-testing RAM interface determines whether data is correct by utilizing an error correction code.

36. (Original) The method of claim 35 wherein the self-testing RAM interface corrects incorrect data by retrieving a copy of the data from another data source.

37. (Original) The method of claim 36, wherein the data source is a magnetic disk drive.

38. (Original) The method of claim 36, wherein the data source is cache memory.

39. (Original) The method of claim 36, wherein the data source is one or more standard RAM devices.

40. (Original) The method of claim 39, wherein the RAM devices contain internal flaws such that the device is not fit for ordinary use.

41. (Original) The method of claim 34, wherein the self-testing RAM interface determines whether data is correct by retrieving a copy of the data from another storage device and comparing the retrieved data and the copy.

42. (Original) An article of manufacturing comprising a computer usable medium having computer readable program code means thereon to perform the method of claim 34.

43. (Previously Presented) The system of claim 1, wherein upon computer system start-up, the self-testing RAM interface effectuates all testing procedures to make portions of tested RAM available to the CPU while the CPU concurrently runs boot process.